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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,331	ASAMI ET AL.	
	Examiner	Art Unit	
	Michael T. Hess	3709	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/07/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 24-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 24-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 8-10, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in the section titled BACKGROUND ART in view of US Pat. No. 4,604,160 to Murakami, et al. (Murakami) and Japanese Pub. No. 05-055758 to Matsushita Electric (Matsushita).

In Reference to Claim 1

The AAPA teaches the following elements of claims 1:

A method for manufacturing a device-incorporated substrate having an insulating layer, a conductor pattern thereon, a void section formed therein, and an electric device housed in said void section and connected to said conductor pattern, said method comprising (AAPA, Fig. 13A-13F):

a void section forming step of forming a void section in said insulating layer (AAPA p. 2, Lines 30-31);

a pattern forming step of forming said conductor pattern on a one surface of a transfer sheet (AAPA P. 3, Lines 3-4) made of metal;

a pattern transfer step of adhering said transfer sheet and said insulating layer each other with said conductor pattern therebetween (AAPA P. 2-3), and removing said transfer sheet; and

a device housing step of housing said electric device within said void section, with said electric device connected to said formed conductor pattern (AAPA P. 3, Lines 13-25).

However, the AAPA fails to disclose and is silent as to the inclusion of a metal transfer sheet and the removal of the transfer sheet including a step of partially dissolving the transfer sheet after forming a seal resin layer between conductor pattern and electric device.

Murakami explicitly teaches a metal transfer sheet (Column 2, Lines 4-14; Column 4, Lines 25-28) and the removal of the transfer sheet (Ref. #s 1 and 6; Col. 5, Lines 58-64), at least partially by dissolving the transfer sheet (Column 2, Lines 12-13; see Columns 5-6, Lines 64-3 and Figure 2).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have used the explicitly taught steps of plating a metal transfer sheet; transferring the plated pattern to a substrate, and removing the metal transfer sheet as in Murakami, in order to produce extremely thin, highly accurate and delicate printed boards, which have high circuit density. (Murakami Columns 3-4, Lines 68-3).

Matsushita explicitly teaches forming a seal resin layer between the conductor pattern and the electric device (paragraph 9, lines 6-8).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have used the explicitly taught use of a seal resin layer between the conductor pattern and the electric device to enhance the productivity of multilayer boards. (Matsushita, Paragraph 7).

In reference to Claim 2

Murakami further teaches:

The method for manufacturing a device-incorporated substrate as described in claim 1, characterized in that:

said transfer sheet comprises a metallic base (Ref. # 1) and a disolvee metal layer (Ref. # 6) that is layered so as to be separable with respect to said metal base material (Ref. # 1) and onto which said conductor pattern is formed (Murakami Column 2, Lines 4-14; Column 4, Lines 25-28; Col. 5, Lines 58-64); and

removal of said transfer sheet includes a step of separating and removing said metal base material from said dissolvee metal layer, and a step of dissolving and removing said dissolvee metal layer (Murakami Column 2, lines 4-14; Column 4, Lines 25-28; Col. 5, Lines 58-64).

In Reference to Claim 3

Murakami further teaches:

The method for manufacturing a device-incorporated substrate as described in claim 1, characterized in that:

said pattern forming step is done by an electroplating method (Murakami Column 2, Lines 7-9).

In Reference to Claim 4

Murakami further teaches:

The method for manufacturing a device-incorporated substrate as described in claim 1, characterized in that:

said pattern forming step includes a step of forming a conductor pattern on one surface of said transfer sheet and a step of burying an insulating material in the gaps in said formed conductor pattern and of flattening said surface of said transfer sheet (Murakami Column 4, Lines34-35).

In Reference to Claim 5

Murakami further teaches

The method for manufacturing a device-incorporated substrate as described in claim 1, characterized in that:

an adhesive material is applied onto one surface of said insulating layer in advance in said pattern transfer step (Murakami Column 2, Lines 17-20).

In Reference to Claim 6

The AAPA and Matsushita further teaches:

The method for manufacturing a device-incorporated substrate as described in claim 1, characterized in that:

said device housing step includes a step of adhering said transfer sheet and said insulating layer to each other (AAPA P. 2, Lines 10-18), and thereafter

housing said electric device into said void section and connecting said electric device to said conductor pattern (Matsushita Paragraph 9, Lines 6-8).

In Reference to Claim 8

Murakami further teaches:

The method of manufacturing a device-incorporated substrate as described in claim 2, characterized in that:

said dissolvee metal layer and said conductor pattern are made of different metal material and said step of dissolving and removing said dissolvee metal layer is done by using an etchant which is able to dissolve said disolvee metal layer but is unable to dissolve said conductor pattern (Murakami Column 4, Lines 35-37).

In Reference to Claim 9

The AAPA further teaches:

The method for manufacturing a device-incorporated substrate as described in claim 1, characterized in that:

said void forming step includes a step of forming a through hole together with said void section, for connecting both surfaces of said insulating layer, and a step of filling conductive material into said through hole (AAPA P. 2-3, Lines 31-3).

In Reference to Claim 10

The AAPA further teaches:

The method for manufacturing a device-incorporated substrate as described in claim 9, said method characterized by further comprising:

layering said formed device-incorporated substrates multiply {sic} with electric connection at said through hole, after said step of filling conductive material (BACKGROUND ART p. 2. lines 19-21.

In Reference to Claim 26

The method for manufacturing a device-incorporated substrate as described in claim 2, characterized in that said dissolvee metal layer is formed to a thickness of 5 micrometers or less (Murakami discloses a range of 1-10 micrometers for the thickness of the metallic film 6, see MPEP 2144.05 – Overlap of Ranges).

In Reference to Claim 27

The method for manufacturing a device-incorporated substrate as described in claim 26, characterized in that said metal base layer is formed to a thickness substantially larger than said dissolvee metal layer in order to provide rigidity to the transfer sheet (Fig. 2(b), metal base 1 is substantially larger than metallic film 6).

3. Claims 24 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Murakami and Matsushita as applied to claim 2 above, and further in view of U.S. Patent No. 6,532,651 to Andou et al. (Andou).

In Reference to Claim 24

The method of manufacturing a device-incorporated substrate as described in claim 2, characterized in that said transfer sheet further comprises an adhesive resin (Andou, Col. 16, Lines 24-25; adhesive foaming agent 24) formed between said metallic base and said dissolvee metal layer.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the adhesive foaming agent of Andou in the method of manufacturing a device-incorporated substrate of AAPA, Murakami and Matsushita in order to facilitate adhering the base material, whether PET or metal, to a film and the subsequent separation of the base material and film as implicitly taught by Andou.

In Reference to Claim 28

The method for manufacturing a device-incorporated substrate as described in claim 2, characterized in that said transfer sheet further comprises a heat foaming layer (Andou, Col. 16, Lines 24-25; adhesive foaming agent 24) formed between said metallic base and said dissolvee metal layer.

4. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Murakami and Matsushita as applied to claim 1 above, and further in view of U.S. Patent Application # 20030178227 A1 to Takahiro et al. (Takahiro).

In Reference to Claim 25

The method for manufacturing a device-incorporated substrate as described in claim 1, characterized in that said transfer sheet is at least 100

micrometers thick (Takahiro, ¶ [0113], Line 1) in order to provide rigidity to the transfer sheet (Takahiro, ¶ [0113], Lines 2-).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the thickness suggestions for the transfer sheet as in Takahiro in the method of manufacturing a device-incorporated substrate of AAPA, Murakami and Matsushita in order to have a properly rigid transfer sheet as explicitly taught by Takahiro.

Response to Arguments

5. Applicants' arguments filed on June 6, 2007 have been fully considered but they are not persuasive.

In Reference to Applicants' Argument That Murakami Must be Withdrawn as a Reference

As applicant inaccurately states that Murakami teaches the removal of transfer sheet 1, 6 prior to transferring the conductor pattern 3 to the insulating film 4, 5. To further clarify Examiner's rejection, I have cited to Col. 5, Lines 58-64, which discuss removing the transfer sheet after applying insulator to the pattern. Thus, Applicants' argument that Murakami should be removed as a reference is not persuasive.

In Reference to Applicants' Argument That Cited References Fail to Teach All Elements of Claim 2

Applicants' urge that the cited references must show removal of both the base material and the disolvee material after attaching pattern to the insulating layer.

Applicants claim removal of the transfer sheet after attaching conductor pattern to said insulating layer. Murakami is consistent with Applicants' claims because complete removal of the transfer sheet 1, 6 is completed after attaching conductor pattern to said insulating layer. Thus, Applicants' argument that the cited references fail to show removal of both the base material after attaching pattern to the insulating layer is irrelevant and not persuasive because Applicants fails to claim that removal of any portion of the transfer sheet must take place after attaching pattern to insulating layer.

In Reference to Applicants' Argument That Cited References Fail to Show Forming an Adhesive Layer on Insulating Layer Prior to Pattern Transfer Step

Applicants' make the blanket argument that the cited references fail to show all limitations of Claim 5. However, Examiner cited **(Murakami Column 2, Lines 17-20)** in his non-final office action which states: "The insulating substratal material may have adhesive agent applied in advance on the surface thereof to which the aforementioned transfer is effected." Thus, Applicants' argument that the cited references fail to show all limitations of Claim 5 is not persuasive.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael T. Hess whose telephone number is 571-270-1994. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Bomberg can be reached on 571-272-4922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MTH

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PRIMARY PATENT EXAMINER